EE 142
Digital Systems

Textbook: *Digital Design* by Morris Mano 4th Edition . This edition contains an introduction to Verilog HDL..
Instructor: Burak Acar (acarbu@boun.edu.tr)
Teaching Assistant: Engin Afacan (engin.afacan@gmail.com)
Webpage: www.vavlab.ee.boun.edu.tr -> Courses -> EE142
Hours: Wednesday 14:00-16:00 TESLA
Grading:

2 projects : 15 % each
2 midterms (in-class) : 20 % each
Midterm 1: 20.10.11
Midterm 2: 15.12.11
Final Exam (in-class) : 30 %

Course Description:
EE 142 is an introductory course to digital design. Its objective is to get familiarize with the fundamentals of digital logic and present the basics of designing circuits involving primarily digital components.
The first four weeks of the course is devoted to the theoretical foundations of digital circuits – namely Boolean algebra. Following in the next three weeks, fundamental combinational components like adders, subtractors and muxes are taught. Derivation of I/O functions and generation of timing diagrams are studied. In the next stage, sequential components starting with simple latches are investigated. In this stage, different sequential components such as flip flops, counters, and finite state machines are studied. Memory units and programmable logic arrays are discussed.
This course does not have laboratory sessions. The laboratory class for this subject is EE240, which is offered also on spring semesters. However, in this class you will learn and use Computer Aided Design (CAD) tools. There will be assignments and projects that will give the ability to use CAD tools to design and simulate digital circuits.

Projects:
Please note that all the projects require you to use Xilinx's Integrated Software Environment (ISE). This software is available online and its limited version is free (Xilinx ISE WebPACK http://www.xilinx.com/ise/logic_design_prod/webpack.htm). You can also get a copy of it on CD or DVD from the lab manager of the Network and Electrical Measurement Laboratory. In case you experience difficulties, please refer to the Installation Guide. You may need to add the Modelsim Library which is available in zipped format. A User's Guide that explains the basic steps of using Project Navigator is also available.
You will be asked to give a demo of your simulation to your TA in a prescheduled manner as well as a hardcopy of it.

Guidelines for Writing Project Reports
Please refer to Report Writing Guidelines for a detailed discussion regarding how to prepare a report. A report template (in pdf or in doc) is also available. The report should

contain a short and clear description of your design – including a short description of your problem (inputs and the required outputs), the steps you took in finalizing your implementation and results from sample inputs if asked to do so. You may look at a sample project report from former years. Please make sure that you use only your own sentences. If you need to use sentences or information (anything such as knowledge, circuit drawings, pictures, graphics) from external source, make sure that you refer to them by using the following conventions:
Place where you use somebody else's work [XXX] where XXX specifies the number of your reference
"…….. sentence of somebody else ….." [YYY] where YYY specifies the number of your reference
At the end of your report, you then add a section named **References** and list all the references, given full information such as who said, where, when, what pages, what html etc. as follows:
References
[XXX] ……Mano, M. Digital Design, pp: 140-142, Addison-Wesley, 1999.
[YYY] http://www.ee.boun.edu.tr
(These are examples to give you the idea!)

Project Demos: You should bring a printed copy of the Project Sheet to your demo session and send your Project Files to boun.ee142@gmail.com (please do not send them to TA's e-mail address) before the project deadlines. Unless otherwise assigned, each student should do his or her homework alone. Please note that in case of any indication of sharing, you will be subject to the EE Department codes for violation of this rule.

Cheating and Plagiarism
Cheating and plagiarism will be treated without tolerance whenever found. Students may discuss assignments/projects with each other but, for grading, must hand in their individual version which means that each student writes down *his/her version with his/her own expressions*.
Topics:

1. Week 1 (28.09.11): Representation and Number Systems (CHs: 1.1-1.9)
2. Week 2 (05.10.11): Boolean Algebra and Logic Gates (CHs: 2.1-2.7, 3.1-3.3)
3. Week 3 (12.10.11): Simplification (CHs: 3.5-3.9)
4. Week 4 (19.10.11): **Midterm 1 on 20.10.2011 (Project 1 assignment)**
5. Week 5 (26.10.11): Combinational Logic (CHs: 4.1-4.5)
6. Week 6 (02.11.11): Combinational Logic (CHs: 4.6-4.8)
7. Week 7 (16.11.11): Combinational Logic (CHs: 4.9-4.11) **(Project 1 demos)**
8. Week 8 (23.11.11): Synch. Seq. Logic (CHs: 5.1-5.4) **(Project 2 assignment)**
9. Week 9 (30.11.11): Synch. Sequential Logic (CHs: 5.5)
10. Week 10 (07.12.11): Synch. Sequential Logic (CHs: 5.7-5.8)
11. Week 11 (14.12.11): **Midterm 2 on 15.12.2011**
12. Week 12 (21.12.11): Registers and Counters (CHs: 6.1-6.3) **(Project 2 demos)**
13. Week 13 (28.12.11): Registers and Counters (CHs: 6.4-6.5)